System Design Using IC Cores; Design, Test and Sign-Off

Prelude:

Core-based designs are becoming common due to increased complexity of systems and a drive to reuse previous design efforts. Core-based designs represent a special challenge in almost all aspects of IC/System design because of the requirements to integrate diverse components with little or no modifications to individual block or core cells. Tools and methodologies are needed for design and validation. This tutorial is devoted to understanding of the issues related to core design, test and use.

Presenters:

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- Ramsey Haddad, Advanced Technology Group, Synopsys Inc., 700 E. Middlefield Ave., Mountain View, CA 94043. (415) 528-4780 / (415) 694-1626 (fax) *haddad@synopsys.com*
- Rob Roy, C&C Research Laboratories, NEC USA Inc., 4 Independence Way, Princeton, NJ 08540. (609) 951-2976/ (609) 951-2499 (fax) *roy@ccrl.nj.nec.com*

Tutorial Outline and Slides

Important Notice:

Welcome (activex)

Introduction to Embedded Cores (activex)
- What are cores?
- Where to use cores?
- Who are the core players?

Design for Test of Core-Based Systems (activex)
- Testing problem of cores and core-based designs
- Designing cores for testability
- Some proposed methodologies - BIST, scan, and boundary scan - their pros and cons

System Validation (activex)
- Validation strategies
- Simulation basics
- Co-Simulation
- Emulation

Reusable Components/Blocks: User Experiences (activex)

The Future (activex)
- Cores as a vehicle for IP-content: CAD tool requirements

Core BookMarks:

IP Suppliers

Summary list can be found for: Hard cores Soft cores and DSP guides.

- Advanced Risc Machines (ARM)
- Synopsys
  - 8051
  - "IBM and Synopsys Team To Support Desktop Design of Complex Systems on a Chip"
- Mentor Graphics
  - Inventra
  - "Synopsys, Mentor Graphics Forge Design Reuse Partnership"
- LSI Logic
  - CoreWare
- Virtual Chips
  - Synthesizable Cores
- Altera
  - MegaCores
- Xilinx
  - CORE Generator Tool for PCI

Services

- Berkeley Design Technology, Inc.

Magazines

- Integrated System Design
  - "Soft cores and USB specs" discussion group
  - "Reusable IP" discussion group
  - "Synthesizable core prices" discusion group
- Virtual Chip Design
  - Hardware-Based Megacells and Cores
  - Software-Based Megacells and Cores

Standards Organizations

- VSIA: Virtual Sockets Interface Alliance

- RAPID: Reusable Application-Specific Intellectual Property Developers

Articles

- "The Evolution of Core + ASIC Methodology" by Julie Cohen Druckerman, Ram Kelkar, Ted Lattrell, Don Pierson, Ann Marie Rincon, and David R. Stauffer

Miscellaneous

i-Logix Inc. - Systems Design Automation Tools - CAD ASIC VHDL
Design Automation Cafe
Embedded Systems Internet -- Resource Page
Design SuperCon97
Motorola Defines ColdFire Core Again
Verilog & EDA Web Page
VHDL Tutorial
Networked Computer Science Technical Reports Library
Routing/Interconnection Network Research Sites
Stanford University CS Electronic and Technical Reports Library
Embedded Systems Conference HomePage
TechWeb --The Technology Super Site
CPU Info Center
IEEE Cores Requirements Survey
DesignCon98

Bibliography: Test Issues

"Test Methodolgy for Embedded Cores which Protects Intellectual Property", K. De, IEEE VLSI Test Symposium, 1997, pp. 1-6.

"Partial Isolation Rings for Testing Embedded Cores", IEEE VLSI Test Symposium, 1997, pp. 7-13.

"Hierarchical Test Assembly for Macro Based VLSI Design," J. Leenstra and L. Spaanenburg, International Test Conference, 1990, pp 520-529.

"A Framework and Method for Hierarchical Test generation," J. D. Calhoun and F. Brglez, IEEE Transactions on Computer-Aided Design, pp 45-67, January 1992.

"Macro Testability; The Result of Production Device Application, F. Bouwan et. al., International Test Conference 1992, pp 232-241

"A Hierarchical Test Pattern Generation System Based on High-Level Primitives," T. M. Sarfert et al, IEEE Transaction on Computer-Aided Design, pp 34-44, January 1992.

"Hierarchical Test Generation under Intensive Global Functional Constraints," J. Lee and J. H. Patel, Design Automation Conference, 1992, pp 261-266.

"Hierarchical Test Generation Using Precomputed Tests for Modules," B. T. Murray and J. P. Hayes, International Test Conference, 1988, pp 221-229.

"MATEG: A Hierarchical Test Generator for Module-Based Circuits,"

D. R. Chiang and Michal Cutler, Fifth Annual IEEE ASIC Conference and Exhibit, 1992, pp 491-494.

"Hierarchical Test Generation: Where We Are, And Where We Should Be Going," J. R. Armstrong, European Design Automation Conference, 1993, pp 434-439.

"Explicit Fault Modeling and Hierarchical Test Pattern Generation in the KARATE System," G Alfs, R. Hartenstein and A. Wodtko, Microprocessor & Microprogramming, August 1989, pp 675-680.

"Managing ASIC IP Throughout Product Life Cycles", D. Crate, On-Chip System Design Conference, Design Supercon, 1997, pp S231-1 through S231-14.

"Design Envrionment for System-on-a-Chip", C. Cherichetti et al, On-Chip System Design Conference, Design Supercon, 1997, pp S312-1 through S312-25.

"Business and Legal Challenges in the Emerging Systems on a Chip Market", P. Lippe, The Intellectual Property in Electronics Conference and Exhibition, 1997, pp 82-100.

Bibliography: Standards and IP Issues

"VSI Alliance Architecture Document", version 1.0, 1997.

"VSI Alliance Roadmap", version 1.0, 1997.

Annotated Bibliography: Research Perspective

Important Notice:

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rgupta@ics.uci.edu

Last updated: Thu May 15 17:40:31 PDT 1997

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      Set      Items   Description
      S1          41   AU=(BOYLAN, S? OR BOYLAN S?)
      S2          52   AU=(COBURN, D? OR COBURN D?)
      S3          23   AU=(CREEDON T? OR CREEDON, T?)
      S4          39   AU=(DEPAOR D? OR DEPAOR, D? OR DE PAOR D? OR DE PAOR, D?)
      S5           2   AU=(GAVIN V? OR GAVIN, V?)
      S6         183   AU=(HYLAND K? OR HYLAND, K?)
      S7        2387   AU=(HUGHES S? OR HUGHES, S?)
      S8         445   AU=(JENNINGS K? OR JENNINGS, K?)
      S9           4   AU=(LARDNER M? OR LARDNER, M?)
      S10       1019   AU=(WALSH B? OR WALSH, B?)
      S11       4191   S1 OR S2 OR S3 OR S4 OR S5 OR S6 OR S7 OR S8 OR S8 OR S10
      S12         17   S11 AND (FPGA OR SOC OR (LAB OR SYSTEM OR COMPUTER)()"ON"(-
                       W)(CHIP OR CHIPS) OR VLSI OR VHSIC OR PLD OR LOGIC()DEVICE? OR
                        GATE()ARRAY?)
      S13         18   S11 AND (FPGA? OR SOC OR SOCS OR (LAB OR SYSTEM OR COMPUTE-
                       R)()"ON"(W)(CHIP OR CHIPS OR CIRCUIT) OR VLSI OR VHSIC OR LOG-
                       IC()DEVICE? OR GATE()ARRAY? OR LARGE()SCALE()INTEGRATION)
      S14        679   S11 AND (CAD OR CAE OR COMPUTER()AIDED()(DESIGN? OR ENGINE-
                       ER?) OR ARCHITECTUR? OR SIMULATION? OR MODEL?)
      S15         10   S13 AND S14
      S16          8   RD (unique items)
      File   2:INSPEC 1969-2004/Jul W2
               (c) 2004 Institution of Electrical Engineers
      File   6:NTIS 1964-2004/Jul W3
               (c) 2004 NTIS, Intl Cpyrght All Rights Res
      File   8:Ei Compendex(R) 1970-2004/Jul W2
               (c) 2004 Elsevier Eng.  Info. Inc.
      File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jul W2
               (c) 2004 Inst for Sci Info
      File  35:Dissertation Abs Online 1861-2004/May
               (c) 2004 ProQuest Info&Learning
      File  65:Inside Conferences 1993-2004/Jul W3
               (c) 2004 BLDSC all rts. reserv.
      File  94:JICST-EPlus 1985-2004/Jun W4
               (c)2004 Japan Science and Tech Corp(JST)
      File 148:Gale Group Trade & Industry DB 1976-2004/Jul 21
               (c)2004 The Gale Group
      File 111:TGG Natl.Newspaper Index(SM) 1979-2004/Jul 20
               (c) 2004 The Gale Group
      File 636:Gale Group Newsletter DB(TM) 1987-2004/Jul 21
               (c) 2004 The Gale Group
      File 275:Gale Group Computer DB(TM) 1983-2004/Jul 21
               (c) 2004 The Gale Group
      File 647:CMP  Computer Fulltext 1988-2004/Jul W2
               (c) 2004 CMP Media, LLC
      File 674:Computer News Fulltext 1989-2004/Jun W4
               (c) 2004 IDG Communications
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16/5/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

02995944 INSPEC Abstract Number: B87065643, C87062070
Title: Good CAD **usage facilitates ambitious designs (** gate arrays **)**
Author(s): **Creedon, T.**
Author Affiliation: Digital Equipment Corp., Clonmel, Ireland
Journal: Microelectronics Journal vol.18, no.3 p.5-21
Publication Date: May-June 1987 Country of Publication: UK
CODEN: MICEB9 ISSN: 0026-2692
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The author aims to show that ambitious designs are made possible using **computer - aided design** (**CAD**) facilities. This is illustrated by means of a recent design example. The purpose of the paper is to encourage designers to take the risk of tackling complex designs, and to show how good **CAD** usage makes it possible to succeed. (1 Refs)
Subfile: B C
Descriptors: cellular arrays; circuit layout **CAD** ; logic **CAD**
Identifiers: **gate array** design; complex designs; **CAD** usage
Class Codes: B1130B (Computer-aided circuit analysis and design); B1265B (Logic circuits); C5210B (Computer-aided logic design); C7410D (Electronic engineering)

16/5/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

02636639 INSPEC Abstract Number: B86021769, C86020415
Title: A technique for distributed execution of design automation tools
Author(s): **Hughes, S.C.** ; Lewis, D.B.; Rimkus, C.J.
Author Affiliation: IBM Corp., Kingston, NY, USA
Conference Title: 22nd ACM/IEEE Design Automation Conference Proceedings 1985 (Cat. No.85CH2142-8) p.23-30
Publisher: IEEE, New York, NY, USA
Publication Date: 1985 Country of Publication: USA xviii+838 pp.
ISBN: 0 8186 0635 5
U.S. Copyright Clearance Center Code: 0738-100X/85/0000-0023$01.00
Conference Sponsor: IEEE; ACM
Conference Date: 23-26 June 1985 Conference Location: Las Vegas, NV, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The demand for computing resources to support design automation systems is growing dramatically due to **VLSI** design considerations. This demand has created a need for multiple computing systems to handle the escalated execution requirements of today's design automation tools. A distribution technique for executing such tools on multiple computing systems is discussed. The Technique uses the definition of three execution modes: interactive foreground, dissociative foreground, and batch. Cost and performance considerations are analyzed as they relate to the overall design automation system as well as individual job executions. An implementation of this technique is presented, including the treatment of common system interface, data management, and job submission techniques. (10 Refs)
Subfile: B C
Descriptors: circuit **CAD** ; distributed processing; **VLSI**
Identifiers: distributed execution; design automation tools; computing resources; **VLSI** ; multiple computing systems; distribution technique; interactive foreground; dissociative foreground; batch; performance considerations; common system interface; data management; job submission techniques
Class Codes: B1130B (Computer-aided circuit analysis and design); B2570 (Semiconductor integrated circuits); C7410D (Electronic engineering)

16/5/7 **(Item 1 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)

03208299 E.I. Monthly No: EI9109108084

Title: High-performance standard cell library and modeling **technique for differential advanced bipolar current tree logic.**

Author: Greub, Hans J.; McDonald, John F.; **Creedon, Ted** ; Yamaguchi, Tadanori

Corporate Source: Center for Integrated Electron, Rensselaer Polytech Inst, Troy, NY, USA

Source: IEEE Journal of Solid-State Circuits v 26 n 5 May 1991 p 749-762

Publication Year: 1991

CODEN: IJSCBC ISSN: 0018-9200

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications); X; (Experimental)

Journal Announcement: 9109

Abstract: A high-performance standard cell library for the Tektronix advanced bipolar process GST1 has been developed. The library is targeted for the 250-MIPS (million instructions per second) fast reduced instruction set computer (FRISC) project. The GST1 devices have a minimal emitter size of 0.6 mu m multiplied by 2.4 mu m and a maximum f//t of 15.5 GHz. By combining advanced bipolar technology and high-speed differential logic, gate propagation delays of 90 ps can be achieved at a power dissipation of 10 mW. The fastest buffers/inverters have a propagation delay of only 68 ps. A 32-b ALU (arithmetic and logic unit) partitioned into four slices can perform an addition in 3 ns using differential standard cells with improved emitter-follower outputs and fast differential I/O drivers. A **modeling** technique for high-speed differential current tree logic is introduced. The technique gives accurate timing information and **models** the transient behavior of current trees. 17 Refs.

Descriptors: LOGIC DESIGN--*Computer Aids; **LOGIC DEVICES** --Gates; COMPUTER **ARCHITECTURE** --Reduced Instruction Set Computing

Identifiers: STANDARD CELL LIBRARY; BIPOLAR CIRCUITS; DIGITAL CIRCUITS

Classification Codes:

721 (Computer Circuits & Logic Elements); 723 (Computer Software); 722 (Computer Hardware)

72 (COMPUTERS & DATA PROCESSING)

Set	Items	Description
S1	862439	CAD OR CAE OR COMPUTER()AIDED()(TOOL? OR ENGINEER?) OR DESIGN? OR ARCHITECTUR? OR SIMULAT? OR MODEL?
S2	30105	VLSI OR FPGA? OR SOC OR SOCS OR (LAB OR SYSTEM OR COMPUTER)()"ON"(W1)(CHIP OR CHIPS) OR VHSIC OR LOGIC()DEVICE? OR GATE()ARRAY? OR LARGE()SCALE()INTEGRAT?
S3	6096	(SHARE? OR DISTRIBUT? OR COMBIN?)(N)(MEMOR? OR STORAGE? OR SRAM OR ROM OR PROM OR EPROM)
S4	4408982	INTERCONNECT? OR PIP OR PIPS OR CONNECT? OR EXCHANG? OR CORE? OR TRANSFER()PATH? OR CONNECT? OR BUS OR BUSES
S5	1902665	LIBRAR? OR GROUP? OR STORED OR SAVE? OR REUS? OR RECYCL?
S6	98	(ARBITRAT? OR LEVEL? OR HIERARCH? OR LAYER?)(3N)S3
S7	4425	S1 AND S2
S8	8	S7 AND S3
S9	1854	S7 AND S4
S10	916	S7 AND S5
S11	2	S2 AND S6
S12	168	S1(3N)S2(4N)(S4 OR S5)
S13	9	S1 AND S6
S14	86	S12 AND IC=(G06F-015? OR G06F-017?)
S15	24	S14 AND S4 AND S5
S16	43	S8 OR S11 OR S13 OR S15
S17	42	S16 AND IC=G06F?
S18	42	IDPAT (sorted in duplicate/non-duplicate order)
S19	42	IDPAT (primary/non-duplicate records only)

File 347:JAPIO Nov 1976-2004/Mar(Updated 040708)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200445
(c) 2004 Thomson Derwent

19/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

014977797 **Image available**
WPI Acc No: 2003-038311/200303
XRPX Acc No: N03-029741
Programmable logic device **circuit** design **development method involves implementing selected logic** core **in one bitstream and applying clock signal to logic device based on another bitstream**
Patent Assignee: XILINX INC (XILI-N)
Inventor: PRICE T O
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6453456	B1	20020917	US 2000533091	A	20000322	200303	B

Priority Applications (No Type Date): US 2000533091 A 20000322
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6453456	B1		12	G06F-017/50	

Abstract (Basic): US 6453456 B1
NOVELTY - A **library** of run-time parameterizable logic **cores** is created and a selected logic **core** is implemented in a configuration bitstream, in response to a command including parameters that specify the logic **core** and **core** placement. A clock signal is applied to the logic device based on another bitstream after which states of the selected elements implemented by the logic **core** are reported.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for system for developing circuit design for programmable logic device.
USE - For developing circuit **design** for programmable **logic devices** (PLDs), testing and implementation of logic **cores** on programmable logic device.
ADVANTAGE - Allows the designer to interactively generate a tool configuration bitstream, advance the PLD clock and observes the states of elements in the PLD. The commands are generated in response to user interaction with a graphical or voice driven user interface and the state information provides the user the information on the behavior of the logic **core** .
DESCRIPTION OF DRAWING(S) - The figure shows a flow diagram that illustrates an exemplary design and test flow.
pp; 12 DwgNo 1/8
Title Terms: PROGRAM; LOGIC; DEVICE; CIRCUIT; DESIGN; DEVELOP; METHOD; IMPLEMENT; SELECT; LOGIC; **CORE** ; ONE; BITSTREAM; APPLY; CLOCK; SIGNAL; LOGIC; DEVICE; BASED; BITSTREAM
Derwent Class: T01; U11; U13; U21
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

19/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

014930211 **Image available**
WPI Acc No: 2002-750920/200281
XRPX Acc No: N02-591385
Integrated circuit designing **method e.g. for** VLSI **circuit, involves mapping** groups **comprising** interconnection **points, logic gates and layout characteristics to IC specification**
Patent Assignee: TELAIRITY SEMICONDUCTOR INC (TELA-N); SACHS H (SACH-I); TELERATY SYSTEMS INC (TELE-N)
Inventor: SACHS H G; SACHS H
Number of Countries: 022 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200286771	A1	20021031	WO 2002US12974	A	20020423	200281	B
US 20020184600	A1	20021205	US 2001840747	A	20010423	200301	
EP 1381980	A1	20040121	EP 2002731487	A	20020423	200410	
			WO 2002US12974	A	20020423		

Priority Applications (No Type Date): US 2001840747 A 20010423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200286771	A1	E	30	G06F-017/50	
Designated States (National): JP					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR					
US 20020184600	A1			G06F-017/50	
EP 1381980	A1	E		G06F-017/50	Based on patent WO 200286771
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR					

Abstract (Basic): WO 200286771 A1
NOVELTY - A specification is determined for the integrated circuit (IC) the **groups** comprising **interconnection** points, logic gates and predefined layout characteristics are mapped to the specification, for designing the IC.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Physical representation definition determining method;
(2) Integrated circuit; and
(3) Electronic logic system designing process.
USE - For designing very large scale integrated (VLSI) circuit (claimed) and systems on a chip (SOC).
ADVANTAGE - By mapping the **groups** , enhanced behavior with respect to area, speed and power is provided and thereby the design productivity is increased and the potential for signal cross-talk is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the flowchart of IC designing process.
pp; 30 DwgNo 1/9
Title Terms: INTEGRATE; CIRCUIT; DESIGN; METHOD; VLSI; CIRCUIT; MAP; **GROUP** ; COMPRISE; **INTERCONNECT** ; POINT; LOGIC; GATE; LAYOUT; CHARACTERISTIC; IC; SPECIFICATION
Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): **G06F-009/45**
File Segment: EPI

19/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014890930 **Image available**
WPI Acc No: 2002-711636/200277
XRPX Acc No: N02-561208

System on a chip design generation method for automation of electronic system, involves automatically associating one socket with another socked, based on relationship between respective signature values

Patent Assignee: GARDNER D N (GARD-I); GARNER R E (GARN-I)
Inventor: GARDNER D N; GARNER R E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6446251	B1	20020903	US 99139146	A	19990614	200277 B
			US 2000540784	A	20000331	

Priority Applications (No Type Date): US 99139146 P 19990614; US 2000540784 A 20000331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6446251	B1		14	G06F-017/50	Provisional application US 99139146

Abstract (Basic): US 6446251 B1

NOVELTY - Two sets of terminals of two different **cores** are respectively represented as two sockets having respective signature values. One of the sockets is automatically associated with the other, based on the relationship between the signature values.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Article of manufacture comprising machine-readable medium storing system on a chip design generation program; and

(2) System on a chip design generation apparatus.

USE - For generating a system on a chip (SOC) design for automation of electronic system e.g. chip integrated system.

ADVANTAGE - Provides **designers** with a convenient method to create and describe an **SOC design** independent of **design** flow. Provides a socket-based **design** with **reusable** intellectual property (IP).

DESCRIPTION OF DRAWING(S) - The figures show operational flowcharts of netlist builder and net naming routine, respectively for generating SOC design.

pp; 14 DwgNo 7A, 7B/7

Title Terms: SYSTEM; CHIP; DESIGN; GENERATE; METHOD; AUTOMATIC; ELECTRONIC; SYSTEM; AUTOMATIC; ASSOCIATE; ONE; SOCKET; BASED; RELATED; RESPECTIVE; SIGNATURE; VALUE
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

19/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014890926 **Image available**
WPI Acc No: 2002-711632/200277
XRPX Acc No: N02-561204

Very large scale integrated circuit design functional verification involves categorizing logic of functional blocks or intellectual property cores **into control, memory, register and datapath portions**

Patent Assignee: NOVAS SOFTWARE INC (NOVA-N)
Inventor: HUANG Y; LEE C; TENG C

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6446243	B1	20020903	US 99298320	A	19990423	200277	B

Priority Applications (No Type Date): US 99298320 A 19990423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6446243	B1		11	G06F-017/50	

Abstract (Basic): US 6446243 B1

NOVELTY - One or more logic included in the functional blocks or intellectual property (IP) **cores** , is categorized into a control, memory, register and datapath portions. The logic of the control portion are **grouped** into multiple finite state machines (FSMs) such that the number of interactions among the FSMs is minimized.

USE - For functional verification of **VLSI** circuit **designs** using **reusable** blocks or intellectual property **cores** .

ADVANTAGE - Allows each designer team to proceed with development independent of other **groups** , since block partitioning provides design content in each circuit partition. Violation of intended design functionality can be identified and provided to user, thereby preventing violation from propagating to other areas of subject design. The functionality of the integrated circuit comprising the functional blocks or IP **cores** is verified based on specific rule.

DESCRIPTION OF DRAWING(S) - The figures show the flowchart explaining the block level design and verification process and the partitioning process for creating super FSM **groups** .

pp; 11 DwgNo 5, 6/10

Title Terms: SCALE; INTEGRATE; CIRCUIT; DESIGN; FUNCTION; VERIFICATION; LOGIC; FUNCTION; BLOCK; INTELLIGENCE; PROPERTIES; **CORE** ; CONTROL; MEMORY ; REGISTER; PORTION
Derwent Class: T01; U21
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

19/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014737453 **Image available**
WPI Acc No: 2002-558157/200259
Related WPI Acc No: 2002-558144
XRPX Acc No: N02-441809

Computer-based method for using a library **map during** design **of IP** cores **in programming Field Programmable** Gate Arrays **(FPGAs), uses macros to specify an interface with macro execution utilizing a plurality of** libraries

Patent Assignee: CELOXICA LTD (CELO-N); ALEXANDER J (ALEX-I)
Inventor: ALEXANDER J G L; ALEXANDER J
Number of Countries: 100 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200261631	A2	20020808	WO 2002GB376	A	20020129	200259	B
US 20030033588	A1	20030213	US 2001772710	A	20010129	200314	
AU 2002228174	A1	20020812	AU 2002228174	A	20020129	200427	

Priority Applications (No Type Date): US 2001772710 A 20010129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200261631	A2	E	33	G06F-017/50	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

US 20030033588	A1	G06F-009/44	
AU 2002228174	A1	G06F-017/50	Based on patent WO 200261631

Abstract (Basic): WO 200261631 A2

NOVELTY - A hardware environment might include a central processing unit that may be replaced by a Field Programmable **Gate Array (FPGA)**. A **library** map may be used during **design** of the **cores** , in a method comprising determining a plurality of macros which specify an interface and using one of a plurality of different **libraries** capable of being utilized by the macro during execution of each macro.

DETAILED DESCRIPTION - INDEPENDENT CLAIMs are also included for the following:

(a) A computer program product for using a **library** map during the design of **cores** ; (A system for using a **library** map during the design of **cores** .

USE - For use during **design** of IP **cores** in programming Field Programmable **Gate Arrays (FPGAs)**.

ADVANTAGE - By utilizing a **library** mechanism that is flexible and able to process dynamically configurable software for defining hardware architectures and storing componentized information in a dynamic storage area, the process provides for effective, flexible definition and maintenance of IP **cores** .

DESCRIPTION OF DRAWING(S) - The figure is a schematic diagram of a hardware implementation of a system for using a **library** map to create and maintain IP **cores** effectively.

pp; 33 DwgNo 1/9

Title Terms: COMPUTER; BASED; METHOD; **LIBRARY** ; MAP; DESIGN; IP; **CORE** ; PROGRAM; FIELD; PROGRAM; GATE; ARRAY; SPECIFIED; INTERFACE; MACRO; EXECUTE; UTILISE; PLURAL
Derwent Class: T01; U11; U21
International Patent Class (Main): **G06F-009/44 ; G06F-017/50**
File Segment: EPI

19/5/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014592466 **Image available**
WPI Acc No: 2002-413170/200244
XRPX Acc No: N02-324653
Programmable interconnect **matrix** design **generation method e.g. for** FPGAs **, involves compiling selected heterogeneous PIM layout tiles into PIM layout comprising hierarchical structure**
Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPR-N)
Inventor: GOWNI S P; PATEL A B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6357035	B1	20020312	US 98111003	P	19981204	200244 B
			US 99285931	A	19990402	

Priority Applications (No Type Date): US 98111003 P 19981204; US 99285931 A 19990402
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6357035	B1		6	G06F-017/50	Provisional application US 98111003

Abstract (Basic): US 6357035 B1
NOVELTY - A programmable **interconnect** matrix (PIM) design is generated by selecting heterogeneous PIM layout tiles from several **group** of PIM layout tiles. Selected PIM layout tiles are compiled into a PIM layout comprising hierarchical structure with a leaf cell as a fundamental component.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) PIM **connection** scheme generation method;
(b) PIM **connection** matrix design generation program;
(c) PIM **connection** scheme generation program
USE - For generating programmable **interconnect** matrix (PIM) **design** for complex programmable **logic devices** (CPLDs), field programmable **gate arrays** (FPGAs).
ADVANTAGE - Avoids the prior manual process of mapping **connections** , hence provides faster less-error prone designs.
DESCRIPTION OF DRAWING(S) - The figure illustrates the overall process of producing a PIM layout.
pp; 6 DwgNo 1/2
Title Terms: PROGRAM; **INTERCONNECT** ; MATRIX; DESIGN; GENERATE; METHOD; COMPILE; SELECT; HETEROGENEOUS; LAYOUT; TILE; LAYOUT; COMPRISE; HIERARCHY ; STRUCTURE
Derwent Class: U11; U13; U21
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

19/5/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014403266 **Image available**
WPI Acc No: 2002-223969/200228
Related WPI Acc No: 1998-362988
XRPX Acc No: N02-171438

Gate array **cells configuration for very** large scale integrated **circuit** design , **involves routing** connection **to** gate array **cells in IC layout, based on net** connectivity **patterns from standard cell function** library

Patent Assignee: CIRRUS LOGIC INC (CIRR-N)
Inventor: CHEN T Y; CUI Y; LEE K

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6260177	B1	20010710	US 96769964	A	19961219	200228	B
			US 9879946	A	19980515		

Priority Applications (No Type Date): US 9879946 A 19980515; US 96769964 A 19961219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6260177	B1		20	G06F-017/50	CIP of application US 96769964 CIP of patent US 6031981

Abstract (Basic): US 6260177 B1

NOVELTY - A standard cell netlist is compiled at a transistor level, using which a gate array cell with an equivalent functionality and **connectivity** of a corresponding standard cell, is defined. The cell is placed in a corresponding location of a standard cell in the IC layout. The cell is **connected** based on net **connectivity** pattern to implement predetermined logic functions.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer system.

USE - For design of very large scale integrated circuits, application specific integrated circuits, using CAD.

ADVANTAGE - Allows using the net **connectivity** patterns in a standard cell **library** , to automatically configure gate array cells.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart of the CAD tool used in selecting gate array cells and reconfiguring them.

pp; 20 DwgNo 5/12

Title Terms: GATE; ARRAY; CELL; CONFIGURATION; SCALE; INTEGRATE; CIRCUIT; DESIGN; ROUTE; **CONNECT** ; GATE; ARRAY; CELL; IC; LAYOUT; BASED; NET; **CONNECT** ; PATTERN; STANDARD; CELL; FUNCTION; **LIBRARY**
Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

19/5/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014358517 **Image available**
WPI Acc No: 2002-179218/200223
Related WPI Acc No: 2002-352345; 2002-383457
XRPX Acc No: N02-136327

Shared memory **resource access** arbitration **method in personal computer, involves** arbitrating shared memory **resources access to prevent conflict between** gate arrays

Patent Assignee: CELOXICA LTD (CELO-N); WILSON A (WILS-I)
Inventor: WILSON A
Number of Countries: 096 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020010825	A1	20020124	US 2000219808	P	20000720	200223	B
			US 2000687012	A	20001012		
			US 2000687481	A	20001012		
			US 2001841701	A	20010423		
WO 200208886	A2	20020131	WO 2001GB3243	A	20010719	200223	
WO 200208913	A2	20020131	WO 2001GB3258	A	20010719	200223	
AU 200170874	A	20020205	AU 200170874	A	20010719	200236	
AU 200170884	A	20020205	AU 200170884	A	20010719	200241	

Priority Applications (No Type Date): US 2000219808 P 20000720; US 2000687012 A 20001012; US 2000687481 A 20001012; US 2001841701 A 20010423

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020010825	A1		10	G06F-012/00	Provisional application US 2000219808
					CIP of application US 2000687012
					CIP of application US 2000687481
WO 200208886	A2	E		G06F-009/00	
WO 200208913	A2	E		G06F-013/00	
AU 200170874	A			G06F-009/00	Based on patent WO 200208886
AU 200170884	A			G06F-013/00	Based on patent WO 200208913

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

Abstract (Basic): US 20020010825 A1

NOVELTY - The **gate arrays** are allowed to access shared memory resource during the execution of the operation. The access to the **shared memory** resources, is **arbitrated** to prevent conflict between the **gate arrays** .

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Computer program product for **shared memory** resource access **arbitration** ;

(b) **Shared memory** resource access **arbitrator** system

USE - For **shared memory** resource access **arbitration** in personal computer, UNIX based workstation, also for embedded systems.

ADVANTAGE - Locking the shared memory resource while communication are in progress with the **gate array** , prevents server data from being interleaved with other data, and prevents sound drive from locking access to the shared memory, thus avoids reinitialization of the device drivers on the **gate arrays** .

DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram of hardware implementation.

pp; 10 DwgNo 1/5
Title Terms: SHARE; MEMORY; RESOURCE; ACCESS; ARBITER; METHOD; PERSON; COMPUTER; ARBITER; SHARE; MEMORY; RESOURCE; ACCESS; PREVENT; CONFLICT; GATE; ARRAY
Derwent Class: T01
International Patent Class (Main): **G06F-009/00** ; **G06F-012/00** ; **G06F-013/00**
International Patent Class (Additional): **G06F-013/14** ; **G06F-013/38**
File Segment: EPI

19/5/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014075560 **Image available**
WPI Acc No: 2001-559774/200163
XRPX Acc No: N01-416021
Macros connection **verification system for hierarchical** large scale integrated **circuit** design **technique, compares** connection **between macros of test circuit with** connection **prestored in table**
Patent Assignee: NIPPON DENKI ENG KK (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000340660	A	20001208	JP 99147465	A	19990527	200163	B

Priority Applications (No Type Date): JP 99147465 A 19990527
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000340660	A		15	H01L-021/82	

Abstract (Basic): JP 2000340660 A
NOVELTY - The predefined **connection** between the macros is **stored** in a table. A macro check program mutually compares the **connection** established between the macros of the test circuit with the prestored **connection** in the table and outputs the verification result.
DETAILED DESCRIPTION - The **connection** between the macros is established for the test circuit. INDEPENDENT CLAIMS are also included for the following:
(a) Macros **connection** verification procedure;
(b) Recording medium for storing control program of LSI
USE - For verifying the correctness of the **connection** between the macros in **large scale integrated** circuit in hierarchical **design** technique.
ADVANTAGE - The correctness of the **connection** between macros is verified in a short time since there is no need for number of process to extract only a verification object from network list, number of processes to produce test pattern, and to analyze whether the verification is correctly **connected** from the output pattern.
DESCRIPTION OF DRAWING(S) - The figure shows LSI circuit diagram.
pp; 15 DwgNo 1/16
Title Terms: **CONNECT** ; VERIFICATION; SYSTEM; HIERARCHY; SCALE; INTEGRATE; CIRCUIT; DESIGN; TECHNIQUE; COMPARE; **CONNECT** ; TEST; CIRCUIT; **CONNECT** ; TABLE
Derwent Class: T01; U11; U12
International Patent Class (Main): H01L-021/82
International Patent Class (Additional): **G06F-017/50** ; H01L-029/00
File Segment: EPI

19/5/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013818757 **Image available**
WPI Acc No: 2001-302969/200132
XRPX Acc No: N01-217616
Database for large scale integrated **circuit** designing , **stores data** groups **having different testing process and identical operation separately from cluster data**
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU); MATSUSHITA ELECTRIC IND CO LTD (MATU)
Inventor: ICHIKAWA O; OHTA M; TAKEOKA S
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000315221	A	20001114	JP 99124034	A	19990430	200132	B
US 6615389	B1	20030902	US 2000561342	A	20000428	200359	
TW 526436	A	20030401	TW 2000108236	A	20000428	200366	

Priority Applications (No Type Date): JP 99124034 A 19990430
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000315221	A		12	G06F-017/50	
US 6615389	B1			G06F-017/50	
TW 526436	A			G06F-017/50	

Abstract (Basic): JP 2000315221 A
NOVELTY - The **core** data representing the design data is **grouped** to form cluster data. The data **group** having different test process with identical operation is identified and **stored** separately.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the design procedure of IC.
USE - For failure test evaluation of IC during designing large scale integrated circuit used in memory, processor.
ADVANTAGE - Reduces testing time with simplified procedure due to optimal storage of testing condition data.
pp; 12 DwgNo 1/11
Title Terms: DATABASE; SCALE; INTEGRATE; CIRCUIT; DESIGN; STORAGE; DATA; **GROUP** ; TEST; PROCESS; IDENTICAL; OPERATE; SEPARATE; CLUSTER; DATA
Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): **G06F-011/22** ; H01L-021/82
File Segment: EPI

19/5/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012765416 **Image available**
WPI Acc No: 1999-571544/199948
XRPX Acc No: N99-421188
Single chip integrated circuit distributed shared memory **node for** VLSI **physical** design **automation, telecommunication**
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: BOYLE D B; JONES E R; KOFORD J S; ROSTOKER M D; SCEPANOVIC R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5963975	A	19991005	US 94229924	A	19940419	199948 B
			US 97932042	A	19970917	

Priority Applications (No Type Date): US 94229924 A 19940419; US 97932042 A 19970917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5963975	A		84	G06F-013/00	Cont of application US 94229924

Abstract (Basic): US 5963975 A

NOVELTY - Cache memory has capacity that is sufficiently small to be fit on chip but creates a substantial cache miss rate. The main memory (508) has cache miss resolution period that compensates for cache miss rate and enables the DSM node (500) to operate at predetermined processing speed.

DETAILED DESCRIPTION - The computing unit (502) comprises processor cache memory and cache controller. The node also includes main memory (508) and interconnect controller (518) which connects the node (500) to remote node (522) via communication channel (520). The memory controller (510) interconnects and maintains memory coherency between the processor, cache memory and memory in the remote node. An INDEPENDENT CLAIM is also included for the communication node.

USE - For **VLSI** physical **design** automation, telecommunication network.

ADVANTAGE - The single IC chip enables cache memory and other components of the DSM node to fit on chip without reducing the processing speed. The small and less expensive processor facilitates to increase the number of processor that can operate simultaneously, thus increasing computational efficiency. Enables the capacity or size of the cache memory to be reduced to 32 KB, thus reducing the chip area to 16 mm2. Reduces total chip area to 253 mm2 and reduces the capacity of main memory to 4 MB, main memory to 125 mm2.

DESCRIPTION OF DRAWING(S) - The figure shows the single chip IC DSM node.

DSM node (500)
Computing unit (502)
Main memory (508)
Memory controller (510)
Interconnect controller (518)
Communication channel (520)
Remote node (522)
pp; 84 DwgNo 67/71

Title Terms: SINGLE; CHIP; INTEGRATE; CIRCUIT; DISTRIBUTE; SHARE; MEMORY; NODE; **VLSI** ; PHYSICAL; **DESIGN** ; AUTOMATIC; TELECOMMUNICATION
Derwent Class: T01
International Patent Class (Main): **G06F-013/00**
File Segment: EPI

19/5/26 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012527252 **Image available**
WPI Acc No: 1999-333358/199928
XRPX Acc No: N99-250988
Hierarchical circuit connection **comparison and verification method for** large scale integrated **circuit** designing - **involves comparing** connection **information higher order cell and layout based on** stored connection **comparison result of lower order cell**
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11121625	A	19990430	JP 97278890	A	19971013	199928 B
JP 3148163	B2	20010319	JP 97278890	A	19971013	200125

Priority Applications (No Type Date): JP 97278890 A 19971013
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11121625	A		6	H01L-021/82	
JP 3148163	B2		6	H01L-021/82	Previous Publ. patent JP 11121625

Abstract (Basic): JP 11121625 A
NOVELTY - The comparison of the **connection** information of circuit in higher order cell and layout is performed based on the **stored connection** comparison result of lower order cell. DETAILED DESCRIPTION - The **connection** information circuit of lower order cell and layout is extracted based on which it is detected whether any element in cell is not **connected** by the layout side. The extracted information of the lower order cell and layout are compared by a comparator (20). The **connection** information of the higher order cell and layout is extracted. The block terminal deleting unit (22) deletes the block terminal **connected** to floating element of the lower order cell. The **connection** comparison result of the lower order cell is **stored** in memory (21). An INDEPENDENT CLAIM is also included for describing circuit **connection** comparison verification apparatus.
USE - For comparing and verification of hierarchical circuit **connection** in **large scale integrated** circuit **designing** .
ADVANTAGE - Prevents false **connection** error during comparison of **connection** information of higher order cell by deleting the block terminal from float element of lower order cell. DESCRIPTION OF DRAWING(S) - The figure depicts drawing of circuit **connection** comparison and verification apparatus. (20) Comparator; (21) Memory; (22) Block terminal deleting unit.
Dwg.1/5
Title Terms: HIERARCHY; CIRCUIT; **CONNECT** ; COMPARE; VERIFICATION; METHOD; SCALE; INTEGRATE; CIRCUIT; DESIGN; COMPARE; **CONNECT** ; INFORMATION; HIGH; ORDER; CELL; LAYOUT; BASED; STORAGE; **CONNECT** ; COMPARE; RESULT; LOWER; ORDER; CELL
Derwent Class: T01; U11
International Patent Class (Main): H01L-021/82
International Patent Class (Additional): **G06F-017/50**
File Segment: EPI

19/5/27 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011009447 **Image available**
WPI Acc No: 1996-506397/199650
XRPX Acc No: N96-426643

Scalable multiple level interconnect architecture **for programmable** gate array **- includes logic blocks formed of multiple configurable function generators interfaced to levels of a hierarchical routing network, coupled to sets of bidirectional input/output lines**

Patent Assignee: BTR INC (BTRI)
Inventor: PANI P M; TING B S
Number of Countries: 072 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9635261	A1	19961107	WO 96US5964	A	19960430	199650	B
AU 9657181	A	19961121	AU 9657181	A	19960430	199711	
TW 294812	A	19970101	TW 96105228	A	19960501	199716	
EP 824791	A1	19980225	EP 96915392	A	19960430	199812	
			WO 96US5964	A	19960430		
JP 11505081	W	19990511	JP 96533406	A	19960430	199929	
			WO 96US5964	A	19960430		
KR 99008270	A	19990125	WO 96US5964	A	19960430	200015	
			KR 97707796	A	19971103		
US 6088526	A	20000711	US 95433041	A	19950503	200037	
			US 97951814	A	19971014		
US 6300793	B1	20011009	US 95433041	A	19950503	200162	
			US 97951814	A	19971014		
			US 99377304	A	19990818		
CN 1188569	A	19980722	CN 96194985	A	19960430	200270	
EP 1294098	A2	20030319	EP 96915392	A	19960430	200322	
			EP 200224873	A	19960430		
EP 824791	B1	20031015	EP 96915392	A	19960430	200368	
			WO 96US5964	A	19960430		
			EP 200224873	A	19960430		
DE 69630372	E	20031120	DE 630372	A	19960430	200401	
			EP 96915392	A	19960430		
			WO 96US5964	A	19960430		

Priority Applications (No Type Date): US 95433041 A 19950503; US 97951814 A 19971014; US 99377304 A 19990818
Cited Patents: 1.Jnl.Ref; US 5204556; US 5296759; WO 9410754; WO 9504404
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9635261	A1	E	62	H03K-019/177	
Designated States (National): AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN					
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG					
AU 9657181	A				Based on patent WO 9635261
TW 294812	A			G11C-005/02	
EP 824791	A1	E			Based on patent WO 9635261
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 11505081	W		49		Based on patent WO 9635261
KR 99008270	A			H03K-019/77	Based on patent WO 9635261
US 6088526	A			G06F-015/20	Cont of application US 95433041
US 6300793	B1			H03K-019/177	Cont of application US 95433041
					Cont of application US 97951814
					Cont of patent US 6088526
CN 1188569	A			H03K-019/177	
EP 1294098	A2	E		H03K-019/177	Div ex application EP 96915392
					Div ex patent EP 824791
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
EP 824791	B1	E		H03K-019/177	Related to application EP 200224873

Related to patent EP 1294098
Based on patent WO 9635261

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DE 69630372 E H03K-019/177 Based on patent EP 824791
Based on patent WO 9635261

Abstract (Basic): WO 9635261 A

Tab network **connectors** (410,420,430....470) interface **groups** of configurable function generators and lower and higher levels of **interconnect** . The network also routes a lower level routing line to a higher. This allows a signal to be driven along longer routing lines without requiring all signal drivers to be sufficiently large to drive a signal along the longest.

The routing lines at each level are divided into sets. The routing hierarchy consisting of routing lines, block **connector** tab networks and turn matrices(710), allow the use of a scalable floor plan.

ADVANTAGE - provides fine granularity without a significant increase in configurable function generators

Dwg.7b/16

Title Terms: MULTIPLE; LEVEL; **INTERCONNECT** ; ARCHITECTURE; PROGRAM; GATE; ARRAY; LOGIC; BLOCK; FORMING; MULTIPLE; CONFIGURATION; FUNCTION; GENERATOR; INTERFACE; LEVEL; HIERARCHY; ROUTE; NETWORK; COUPLE; SET; BIDIRECTIONAL; INPUT; OUTPUT; LINE

Derwent Class: U13; U21

International Patent Class (Main): **G06F-015/20** ; G11C-005/02; H03K-019/177 ; H03K-019/77

International Patent Class (Additional): G11C-005/06; H03K-019/173

File Segment: EPI

19/5/40 **(Item 40 from file: 347)**
DIALOG(R)File 347:JAPIO

05476462 **Image available**
MULTIPROCESSOR SYSTEM

PUB. NO.: 09-091262 [JP 9091262 A]
PUBLISHED: April 04, 1997 (19970404)
INVENTOR(s): KAWADA TETSUO
KUROISHI NORIHIKO
KAWACHI KENICHI
MIYAGAWA NOBUAKI
AIHARA REIJI
KOYANAGI MITSUMASA
APPLICANT(s): FUJI XEROX CO LTD [359761] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-264661 [JP 95264661]
FILED: September 20, 1995 (19950920)
INTL CLASS: [6] **G06F-015/177** ; **G06F-013/00** ; **G06F-015/173** ; H04L-012/42
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 44.3 (COMMUNICATION -- Telegraphy); 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS

ABSTRACT

PROBLEM TO BE SOLVED: To provide the system **architecture** and **VLSI** chip **architecture** which realize a high communication performance and a low cost at the time of constituting a **distributed memory** type multiprocessor system by burying the communication function of a ring bus form in a **VLSI** chip constituting a processor element.

SOLUTION: In the multiprocessor system which has a ring type communication network and performs communication in the master slave form, each of processor elements 13a, 17, and 12a is provided with a node ID register, which sets a node ID to each node, and an ID setting flag. When the ID setting flag is reset, the node ID added to a node ID setting instruction is set to the node ID register and the ID setting flag is set to perform such control processing that the node ID setting instruction is not transmitted to nodes below; and when the ID setting flag is set, the control processing is performed to transmit the node ID setting instruction to nodes on the downstream side

19/5/41 (Item 41 from file: 347)
DIALOG(R)File 347:JAPIO

04128672 **Image available**
DESIGNING SYSTEM FOR GATE ARRAY

PUB. NO.: 05-120372 [JP 5120372 A]
PUBLISHED: May 18, 1993 (19930518)
INVENTOR(s): HORIKOSHI KENGO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-305683 [JP 91305683]
FILED: October 25, 1991 (19911025)
INTL CLASS: [5] **G06F-015/60** ; H01L-027/118; H01L-021/82
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R060 (MACHINERY -- Automatic Design); R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)
JOURNAL: Section: P, Section No. 1606, Vol. 17, No. 488, Pg. 140, September 03, 1993 (19930903)

ABSTRACT

PURPOSE: To decrease the man-hours for the generation of a **library** and facili tate the design by decreasing the number of function blocks which should be prepared as the **library** when the **gate array** is **designed** and to shorten the development period by copying with a limitation error and a timing error after circuit designing without reviewing the circuit.

CONSTITUTION: The system has functions (ST-20 and ST-21) which find the best driving ability reinforcement coefficient from the **connection** state of the blocks and output it to a file (size file) 34, a function (ST-22) which reads in the size file, performs delay calculation, and corrects the coefficient so as to match the coefficient with a delay value given from a control card 33 and outputs it to the size file, and functions (ST-27 and ST-28) which read in the size file, generate a driving ability reinforcement pattern (ST-23, ST-24, and ST-25), and lays out the pattern on an LSI chip.

02469075 **Image available**

CAD SYSTEM

PUB. NO.: 63-085975 [JP 63085975 A]
PUBLISHED: April 16, 1988 (19880416)
INVENTOR(s): YAMAMOTO AKIYASU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-232127 [JP 86232127]
FILED: September 30, 1986 (19860930)
INTL CLASS: [4] **G06F-015/60**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS
JOURNAL: Section: P, Section No. 752, Vol. 12, No. 323, Pg. 82, September 02, 1988 (19880902)

ABSTRACT

PURPOSE: To **design** a large scale **gate array** by using a **design** editor extracting and **connecting** a function module required for a **large scale integrated** circuit from a **CAD library**, an input means for respective required information, and a display means for successively display.

CONSTITUTION: The function modules of peripheral circuits 15, 16 corresponding to 82C59, 82C53 more than 10K gate having an equal function to the peripheral circuit of a CPU, peripheral circuits 17-19 corresponding to cascade **connected** 82C37 and a random part 20 are **stored** in the CAD **library** 1. When the respective information of a large scale gate array desired to be designated is inputted to a console 7, the design editor 4 extracts the required module from the CAD **library** 1. The extracted modules are **connected** according to respective design rules **stored** in a design data base 3. The simulation of the circuit is carried out according to the instruction of the console 7. The respective function modules are laid out by a pattern editor 5 and a partial correction is executed. In such a way, a final wiring pattern can be displayed on the screen of a display 6.

Set	Items	Description
S1	1214223	CAD OR CAE OR COMPUTER()AIDED()(TOOL? OR ENGINEER?) OR DESIGN? OR ARCHITECTUR? OR SIMULAT? OR MODEL?
S2	98403	VLSI OR FPGA? OR SOC OR SOCS OR (LAB OR SYSTEM OR COMPUTER)()"ON"(W1)(CHIP OR CHIPS) OR VHSIC OR LOGIC()DEVICE? OR GATE()ARRAY? OR LARGE()SCALE()INTEGRAT?
S3	6599	(SHARE? OR DISTRIBUT? OR COMBIN?)(N)(MEMOR? OR STORAGE? OR SRAM OR ROM OR PROM OR EPROM)
S4	1153403	INTERCONNECT? OR PIP OR PIPS OR CONNECT? OR EXCHANG? OR CORE? OR TRANSFER()PATH? OR CONNECT? OR BUS OR BUSES
S5	914988	LIBRAR? OR GROUP? OR STORED OR SAVE? OR REUS? OR RECYCL?
S6	255	(ARBITRAT? OR LEVEL? OR HIERARCH? OR LAYER?)(3N)S3
S7	1325	S1(10N)S2(10N)(S3 OR S4 OR S5)
S8	2	S2(5N)S6
S9	12	S1(2N)S2(10N)S3
S10	15	S1(4N)S2(10N)S3
S11	24	S1(S)S2(S)S3(S)S4(S)(S5 OR S6)
S12	35	S8 OR S9 OR S10 OR S11
S13	21	S12 AND IC=G06F?
S14	10	S12 AND IC=(G06F-017? OR G06F-015)
S15	10	IDPAT (sorted in duplicate/non-duplicate order)
S16	10	IDPAT (primary/non-duplicate records only)

File 348:EUROPEAN PATENTS 1978-2004/Jul W02
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040715,UT=20040708
(c) 2004 WIPO/Univentio

16/3,K/5 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00986961 **Image available**

TIMING-INSENSITIVE GLITCH-FREE LOGIC SYSTEM AND METHOD

SYSTEME LOGIQUE INSENSIBLE AUX DEFAILLANCES ET AUX PROBLEMES DE SYNCHRONISATION ET PROCEDE ASSOCIE

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Patent and Priority Information (Country, Number, Date):
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Application: WO 2001US25546 20010814 (PCT/WO US0125546)
Priority Application: WO 2001US25546 20010814
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS
LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ
TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 85087

Main International Patent Class: **G06F-017/50**
Fulltext Availability:
Detailed Description

Detailed Description
... for the Simulation system to manage the various memory blocks associated with the configured hardware **model** of the user's **design** , which was programmed into the array of **FPGA** chips in the reconfigurable hardware unit.

The **memory** **Simulation** aspect of the invention provides a structure and scheme where the numerous memory blocks associated...

16/3,K/8 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00750786 **Image available**

SCALABLE MULTI-PROCESSOR SYSTEM FOR REAL TIME APPLICATIONS IN COMMUNICATIONS ENGINEERING

SYSTEME MULTIPROCESSEUR POUVANT ETRE MIS A L'ECHELLE ET DESTINE A DES APPLICATION TEMPS REEL DANS LES TELECOMMUNICATIONS

SKALIERBARES MULTI-PROZESSORSYSTEM FUR ECHTZEITANWENDUNGEN IN DER NACHRICHTENTECHNIK

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Application: WO 2000DE1015 20000403 (PCT/WO DE0001015)
Priority Application: DE 19917815 19990420
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CN DE ID US
Publication Language: German
Filing Language: German
Fulltext Word Count: 2909

International Patent Class: **G06F-015/17**
Fulltext Availability:
Detailed Description

Detailed Description

... im Rahmen einer Evaluierung ergeben,
dass eine Standardlosung mit einem Prozessor und einem gemeinsamen Speicher (**shared memory**) bei weitem nicht den Performance Anforderungen genugt, Durch die Vielzahl von Kompo
nenten, die bei **SoC** (**System on Chip**) **Designs** ublich sind, kommt es im allgemeinen zu langeren Wartezeiten am **shared memory** , da physikalisch langere Wartezeiten am externen Spei
cher entstehen und im weiteren mit Zugriffsbelegungen (bus...

16/3,K/10 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00144529 **Image available**

METHOD AND APPARATUS FOR CIRCUIT SIMULATION USING PARALLEL PROCESSORS INCLUDING MEMORY ARRANGEMENT AND MATRIX DECOMPOSITION SYNCHRONIZATION

PROCEDE ET APPAREIL DE SIMULATION DE CIRCUITS UTILISANT DES PROCESSEURS PARALLELES COMPRENANT UN AGENCEMENT DE MEMOIRE ET UNE SYNCHRONISATION DE DECOMPOSITION MATRICIELLE

Patent Applicant/Assignee:
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Inventor(s):
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GREENBERG Steven,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8801412 A1 19880225
Application: WO 87US2079 19870820 (PCT/WO US8702079)
Priority Application: US 86476 19860820
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AT BE CH DE FR GB IT JP LU NL SE
Publication Language: English
Fulltext Word Count: 4677
Main International Patent Class: **G06F-015/31**
Fulltext Availability:
Detailed Description

Detailed Description
... which operate in
parallel with each other, and closely coupling thb1plurality of processors to a **shared memory** , is a solution to the increasingly complex problem of circuit **simulation** . One such solution is proposed in Jacob, Newton,, and Pederson, "Direct Method Circuit **Simulation** Using Multiprocessors," Proceedings of the International Symposium on Circuits and Systems, May 1986. Another such solution is proposed in White, "Parallelizing Circuit **Simulation** - A Combined Algorithmic and Specialized Hardware Approach, Proceedings of the ICCD, Rye, New York, 1985...

...these references, however, recognizes a
significant drawback to the utilization of parallel processing for circuit **simulation** . Since the processors are sharing the same memory, and the processors are ...computing values for different circuit elements throughout the LSI or
CM IMA=@ @Zfwrt t@z
VLSI circuit, or some defined sub-portion of such circuit, the processors will quite often be...

...processes, which update values for. a given node based on computations relating to circuit elements **connected** to the node, and a memory location within the computer is used to store the...

...any given time for a particular node, the
problem arises that the access to the **shared memory** must be strictly controlled. otherwise, more than one processor may write information into a memory...

...to a
particular node, at the same time another processor is attempting to read previously **stored** information related to that node or write new information relating to that node, based on...

...Jacob et al. paper, noted above, investigates the

parallel implementation of a direct method circuit **simulator** using SPLICE, and using up to eight processors of a **shared** **memory** machine. An efficiently close to forty-five percent S U I 03 S @ T II...

...efficiency is the result of synchronization of the multiple processors in their access to common **shared** **memory** locations.

Parallelization employing such simulation programs as SPICE uses a list of circuit components and...